UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/778,761	02/08/2001	Shigeru Onoya	12732-013001/ US4610	4159

26171 7590 10/18/2005

FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
EISEN, ALEXANDER	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/778,761	ONOYA, SHIGERU	
	Examiner	Art Unit	
	Alexander Eisen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-15 and 18-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,10,12,13,15,20,23-26 and 28-37* is/are allowed.

6)☒ Claim(s) *1-3,6-9,11,14,18,19,21,22 and 27* is/are rejected.

7)☒ Claim(s) *38 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8-1-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6-9, 11, 14, 18, 19, 21, 22 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirakata, US 6,496,172 B1.

With respect to claim 1 Hirakata discloses a method for driving a semiconductor display device wherein display signals input to pixel electrodes in a vertical line have a same polarity and the same polarity is independently controlled for each vertical line of the plurality of pixels, and wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period (FIG. 1A; col. 9, lines 34-67).

In regard to claim 2 Hirakata additionally discloses that the method wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces the flicker (see abstract; col. 5, lines 40-45).

As to claim 3, Hirakata further discloses that the method of driving a semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces vertical striping (col. 10, lines 40-46).

As to claim 6, Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods (compare frame periods 1-4 in FIG. 1A, fore example).

As to claim 7, Hirakata also discloses a semiconductor display device comprising a source signal line driver circuit 105 (FIG. 2); a gate signal driver circuit (104); a plurality of source signal lines 103; a plurality of gate signal lines 102; a pixel portion (display region 106); a display signal generation portion which has a control portion 108, a polarity data signal generation portion 208; a display signal selection portion 109, a + side display signal generation portion 201; a - side display signal generation portion, and wherein display signals input to display electrodes in a vertical line have the same polarity, and the same polarity is independently controlled for each vertical line of the plurality of pixels, and wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period.

As to claim 8, Hirakata additionally discloses that the method wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces the flicker.

As to claim 9, Hirakata further discloses that the method of driving a semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period reduces vertical striping, and wherein the same polarity is independently controlled for each vertical line of the plurality of pixels.

As to claim 11, Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods.

As to claim 14 Hirakata further teaches that the semiconductor display device wherein pixels to which display signals having a particular polarity are input are changed irregularly in a certain fixed period have reduced vertical striping, and polarities of the display signals input to pixel electrodes in a vertical lines change together.

As to claims 18-19, 21-22 and 27 Hirakata further teaches that a polarity of display signals input to only some of the pixel electrodes changes in two adjacent frame periods.

Allowable Subject Matter

3. Claims 4, 10, 12, 13, 15, 20, 23-26 and 28-37 are allowed.

4. The following is an examiner's statement of reasons for allowance: none of the prior art, either singularly or in combination, teach or suggest an arrangement wherein the polarities of the display signals input to the pixel electrodes in a vertical line are changed together in the methods claimed in independent claims 4, 10, 12, 13 and 24.

5. Claims 38 and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims contain a subject matter similar to that of claim 12 and would be allowed on the same grounds.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments with respect to claims 1-3, 6-9, 11, 14, 18, 19, 21, 22 and 27 have been fully considered but they are not persuasive. Applicant argues that Hirakata describes changing the polarity pattern multiple times during the frame period, reciting column 9, lines 29-32 . Examiner respectfully disagrees and submits that the Applicant has misread Hirakata. Hirakata describes that four polarity patterns are displayed sequentially in four frames, each having a different pattern from (1) to (4). See col. 9, lines 34-37; col. 10, lines 7-14 and FIG. 4 showing that four polarity patterns from (1) to (4) are displayed in four sequential frames (FIRST FRAME to FOURTH FRAME in the figure repeating the pattern (1) in FIFTH FRAME and so on). Hirakata compares this method with the traditional one, where only two different patterns are displayed in sequential frames (col. 9, lines 10-15 and FIG. 18). The pattern is maintained during the frame. As to the argument that the pattern is changing irregularly after the frame period, as it was noted earlier the Applicant's view of randomness is not actual random patterns, but quite deterministic and distinct patterns as shown in different embodiments, and the specification states that the number of different patterns should be at least three (page 42 from line 2 downwards). Therefore, while the patterns are distinct and different and look random they are actually pseudorandom and repeat themselves in a certain fixed period of time (could be in three frames, according to the Applicant). Hirakata, in turn, provides four different patterns. In this sense Hirakata's polarity patterns for four frames are not less random than those of Applicant's and as a result the rejection based on Hirakata is maintained.

The arguments related to claims 4, 10, 12, 13, 15, 20, 23-26 and 28-37, as amended, are found to be persuasive and resulted in allowance of claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 11, 2005

Alexander Eisen
Primary Examiner
Art Unit 2674